AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0041] at page 11, line 16 with the following paragraph

[0041] In one embodiment a delay lock loop (not shown) may be used to align the transition edges of the low frequency reference clock 520 with the transition edges of the clock signal which clocks the flip flop 170 of the decision feedback equalizer to ensure that the monitor circuit 505 is properly synchronized with the decision feedback equalizer. A delay lock loop which is suitable for synchronizing the reference clock 520 and the clock [[260]] signal which clocks the flip flop 170 of the decision feedback equalizer is disclosed in commonly owned U.S. Provisional Patent Application Ser. No. 60/531,095 entitled "HIGH FREQUENCY BINARY PHASE DETECTOR", filed Dec. 19, 2003, the disclosure of which is incorporated herein by reference.